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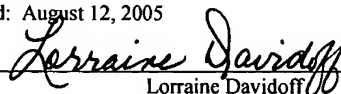
Appl. No. : 10/731,832 Confirmation No. 4396
Applicants : Seyed-Ali Hajimiri, et al.
Filed : December 9, 2003
Art Unit : 2817
Examiner : Khanh V. Nguyen
Docket No. : 13641.0060
Customer No. : 33649

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In accordance with the requirements of 37 C.F.R. §§ 1.97 and 1.98, attached please find Forms PTO/SB/08A and PTO/SB/08B listing information for consideration by the U.S. Patent and Trademark Office in connection with its examination of the above-referenced patent application. A copy of each reference is enclosed herewith.

Applicants submit that no representation is made, and no representation is intended, that more relevant material does not exist, or that the order of presentation of these materials in any way reflects their relative pertinence. The listings on the attached Forms PTO/SB/08A and PTO/SB/08B are not intended to constitute an admission of any kind. Specifically, this presentation is not an admission that any of the items listed are properly citable against the above-identified application as prior art. Applicants respectfully submit that their invention is patentable over the enclosed documents listed on Forms PTO/SB/08A and PTO/SB/08B.

Pursuant to §1.97(e)(1), several items of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart

foreign application more than three months prior to the filing of this information disclosure statement and, therefore, a fee of \$180.00 is believed to be due. Also enclosed are other prior art articles known to Applicants.

Commissioner of Patents and Trademarks is hereby authorized to charge the \$180.00 fee to Deposit Account No. 50-0530. If any applicable fee or refund has been overlooked, the Commissioner is hereby authorized to charge any fee or credit any refund to the deposit account of Godwin Gruber, LLP, No. 50-0530.

Dated: August 12, 2005

Respectfully submitted,

GODWIN GRUBER LLP

By 

Christopher J. Rourk

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Complete if Known

(Use as many sheets as necessary)

Sheet	1	of	4
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Application Number	10/731,832
Filing Date	12/09/2003
First Named Inventor	Sayed-Ali Hajimir
Art Unit	2817
Examiner Name	Khanh V. Nguyen
Attorney Docket Number	13641.0060

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)	MM-DD-YYYY			
		JP 07204367	10-08-1995	Mitsui Yasuro		
		JP 54172531	12-28-1979	Kanemoto Yoshitaka		

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	10/731,832		
		Filing Date	December 9, 2003		
		First Named Inventor	Seyed-Ali Hajimiri		
		Art Unit	2817		
		Examiner Name	Khanh V. Nguyen		
Sheet	2	of	4	Attorney Docket Number	13641.0060

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	International Search Report for PCT/US03/39174, May 5, 2004.	
	2	D.K. SHAEFFER, ET AL., "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," IEEE Journal of Solid-State Circuits, IEEE Inc., May 1997, pp. 745-749, Vol. 32, No. 5, New York, NY.	
	3	H. DARABI, ET AL., "A 4.5-mW 900-MHz CMOS Receiver for Wireless Paging," IEEE Journal of Solid-State Circuits, August 2000, pp. 1085-1096, Vol. 35, No. 8.	
	4	S. WU, ET AL., "A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications," IEEE Journal of Solid State Circuits, December 1998, pp. 2178-2185, Vol. 33, No. 12.	
	5	A. ROFOUGARAN, ET AL., "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver," IEEE Journal of Solid-State Circuits, July 1996, pp. 880-889, Vol. 31, No. 7.	
	6	J.C. RUDELL, ET AL., "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," IEEE Journal of Solid-State Circuits, December 1997,	
		pp. 2071-2088, Vol. 32, No. 12.	
	7	H. SAMAVATI, ET AL., "A 5-GHz CMOS Wireless LAN Receiver Front End," IEEE Journal of Solid-State Circuits, May 2000, pp. 765-772, Vol. 35, No. 5.	
	8	B.A. FLOYD, ET AL., "A 23.8-GHz SOI CMOS Tuned Amplifier," IEEE Transactions on Microwave Theory and Techniques, September 2002,	
		pp. 2193-2196, Vol. 50, No. 9.	

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		Examiner Name	Khanh V. Nguyen		
Sheet	3	of	4	Attorney Docket Number	13641.0060

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	9	P. LEROUX, ET AL., "A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz," IEEE Journal of Solid-State Circuits, June 2002, pp. 760-765, Vol. 37, No. 6.	
	10	S.F. TIN, ET AL., "A Simple Subcircuit Extension of the BSIM3v3 Model for CMOS RF Design," IEEE Journal of Solid-State Circuits, April 2000, pp. 612-624, Vol. 35, No. 4.	
	11	H. HASHEMI, ET AL., "Concurrent Multiband Low-Noise Amplifiers - Theory, Design, and Applications," IEEE Transactions on Microwave Theory and Techniques, January 2002,	
		pp. 288-301, Vol. 50, No. 1.	
	12	B.A. FLOYD, ET AL., "A 15-GHz Wireless Interconnect Implemented in a 0.18 (mu)M CMOS Technology Using Integrated Transmitters, Receivers, and Antennas," 2001 Symposium on VLSI	
		Circuits Digest of Technical Papers, June 2001, pp. 155-158.	
	13	X. GUAN, ET AL., "A 24GHz CMOS Front-end," in Proc. 28th ESSCIRC, September 2002, pp. 155-158.	
	14	S.M. ALAMOUTI, "A Simple Transmit Diversity Technique for Wireless Communications," IEEE Journal on Select Areas in Communications, October 1998, pp. 1451	
		-1458, Vol. 16, No. 8.	
	15	D. LU, ET AL., "A 24-GHz Active Patch Array," International Journal of Infrared and Millimeter Waves, May 2002, pp. 693-704, vol. 23.	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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	Filing Date		December 9, 2003		
	First Named Inventor		Seyed-Ali Hajimiri		
	Art Unit		2817		
	Examiner Name		Khanh V. Nguyen		
Sheet	4	of	4	Attorney Docket Number	13641.0060

NON PATENT LITERATURE DOCUMENTS

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	16	D.K. SHAEFFER, ET AL., "A 1.5V, 1.5GHz CMOS Low Noise Amplifier," 1996 Symposium on VLSI Circuits Digest of Technical Papers, June 1996, pp. 32-33.	
	17	R.S. ELLIOTT, "Beamwidth and directivity of large scanning arrays, first of two parts," Microwave Journal, Dec. 1963, pp. 53-60.	
	18	J.C. LIBERTI, ET AL., "Smart Antennas for Wireless Communications: IS-95 and Third Generation CDMA Application," 1999, pp. 83-88, Prentice Hall, New Jersey.	
	19	Y.C. HO, ET AL., "3 V low noise amplifier implemented using a 0.8 (mu)m CMOS process with three metal layers for 900 MHz operation," Electronic Letters, Jun 1996,	
		pp. 1191-1193, vol. 32, no. 13.	
	20	D.K. SCHAEFFER, ET AL., "The Design and Implementation of Low-Power CMOS Radio Receivers," 1999, pp. 52-67, Kluwer Academic Publishers, Boston.	
	21	Y.C. HO, ET AL., "Implementation and Improvement for RF Low Noise Amplifiers in Conventional CMOS Technologies," 2000, Ph.D Thesis, University of Florida, Florida	
	22	A. VAN DER ZIEL, "Noise in Solid State Devices and Circuits," 1986, pp. 88-91, New York: Wiley.	

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